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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/636,060	08/07/2003	Derick G. Behrends	ROC920030049US1	1005

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Intellectual Property Law Dept.
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EXAMINER	
KERVEROS, JAMES C	
ART UNIT	PAPER NUMBER
2117	

MAIL DATE	DELIVERY MODE
10/02/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/636,060	BEHRENDS ET AL.	
	Examiner	Art Unit	
	JAMES C. KERVEROS	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 September 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☒ Claim(s) *1-12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 9/20/2007 has been entered.

This is a Non-Final Office Action in response to the Amendment filed with the RCE on 9/20/2007. Claims 1-21 are presently under examination and pending.

Response to Arguments

Applicant's arguments filed on 9/20/2007, with respect to claims 1-21, have been fully considered but they are not persuasive.

In reference to the claimed feature of "selecting a bit" under 35 U.S.C. 112, first paragraph rejection, for failing to comply with the enablement requirement that the feature of "selecting a bit" was commonly known in the art well before the time of the invention, Applicant's argument irrelevant, because even if "selecting a bit" is well known in the art, a skilled person would not be able to carry out the invention as a hole, due the lack of an enabling description by the specification. Even, arguendo, Applicant's argument is valid, then "selecting a bit" is prior art, and as such the claimed invention is obvious variation over the prior art.

The claimed invention, which merely recites selecting a bit from a memory array and storing such a bit, is too broad in scope, preempts a 35 U.S.C. 101 Judicial Exception (Abstract Idea, Law of Nature, or Natural Phenomenon), as described below, because the claimed limitations of selecting and storing are not directed to any practical application. In the instant application, merely selecting a bit from a plurality of memory arrays would impermissibly cover every substantial practical application of memory testing and thereby preempt all use of such testing, because inherently, a person of ordinary skill in the art must select a bit during memory read out prior to testing.

The introduction of a new matter into the independent claims, "wherein an outcome of the ABIST test is determined based on the stored selected bit", does not render the claimed invention practical as having "useful, concrete and tangible result." Furthermore, determining the outcome of a test result of a memory under test based on a stored selected bit from the memory could be rather predictable and obvious, depending on the condition of any one the memory cells associated with the selected bit.

In response to Applicant's argument that Jain fails to disclose receiving a bit and storing the selected bit from the selected memory array, clearly the selected faulty BitF from the final test results TR to the BIST control unit generated by the comparator unit 106, as disclosed by Jain, corresponds to the claimed selected bit from the memory, since the comparator unit is a species, which is part a genus the memory array comprising the memory bank 104 and the comparator unit, and as such it anticipates the selected bit. Therefore, the claimed invention fails to distinguish between a bit

selected from a memory unit and a bit selected from a comparator unit, since both units are integral part of the memory array formed on the IC chip 100, Figs. 1-4.

Specification

The specification is objected to under 37 CFR 1.71 because the specification lacks an enabling description for claims 1-3, 6-9, 12, in reference to the limitation "selecting a bit".

Claim Objections

Claims 1-12 are objected to because independent claims 1 and 7 in the preamble recite "a method for testing an integrated circuit (IC)", which has not been given patentable weight because the recitation occurs in the preamble, since the main body of the claims do not include "testing an integrated circuit".

A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951). Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact

terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-12 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The specification lacks enablement with respect to claimed limitation "selecting a bit" recited in claims 1-3, 6-9, 12. The specification fails to clearly describe the claimed invention with respect to selecting a bit from a memory, so a person skilled in the art would be able to carry out the invention.

Claims 1-21 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The specification lacks enabling description because of the introduction of a new matter, "wherein an outcome of the ABIST test is determined based on the stored selected bit" recited in the independent claims 1, 7, 13 and 17. In this case, Applicant's specification merely describes, "storing the selected bit from the selected memory array for each of the first and second plurality of memory arrays". There is no description in

the application as originally file to suggest what kind of effect if any the stored selected bit has on the ABIST test.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1-3, 6-9, 12 recite the limitation "selecting a bit". There is insufficient antecedent basis for this limitation in the claims, because it is not clear whether the selected bit is the same bit or different bits.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 1-12 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Independent Claims 1 and 7 recite a method of testing an integrated circuit IC, including the steps of selecting a bit from each of a plurality of memory arrays, selecting one of plurality of memory arrays, and storing the selected bit. The steps of selecting

and storing constitute an abstract idea without any tangible results, and without further reciting practical applications, such as a structure or apparatus for implementing the steps. The method can be accomplished merely by someone thinking about the recited steps and not actually doing anything, since they do not transform the claimed invention into a statutory process, i.e., one that is a practical application of an abstract idea to produce a useful, concrete and tangible result.

In the instant application, merely selecting a bit from a plurality of memory arrays would impermissibly cover every substantial practical application of memory testing and thereby preempt all use of such testing, because inherently, a person of ordinary skill in the art must select a bit during memory read out prior to testing.

In this case, the Claimed Invention Preempts a 35 U.S.C. 101 Judicial Exception (Abstract Idea, Law of Nature, or Natural Phenomenon), because the claimed limitations are not directed to any practical application. A claimed invention is directed to a practical application of a 35 U.S.C. 101 judicial exception when it: "transforms" an article or physical object to a different state or thing; or otherwise produces a useful, concrete and tangible result.

"Phenomena of nature, though just discovered, mental processes, abstract intellectual concepts are not patentable, as they are the basic tools of scientific and technological work." Benson, 409 U.S. at 67, 175 USPQ at 675. One may not patent a process that comprises every "substantial practical application" of an abstract idea, because such a patent "in practical effect would be a patent on the [abstract idea] itself." Benson, 409 U.S. at 71-72, 175 USPQ at 676; cf. Diehr, 450 U.S. at 187, 209 USPQ at

8 (stressing that the patent applicants in that case did "not seek to pre-empt the use of [an] equation," but instead sought only to "foreclose from others the use of that equation in conjunction with all of the other steps in their claimed process"). "To hold otherwise would allow a competent draftsman to evade the recognized limitations on the type of subject matter eligible for patent protection." Diehr, 450 U.S. at 192, 209 USPQ at 10".

Thus, a claim that recites a computer that solely calculates a mathematical formula (see Benson) or a computer disk that solely stores a mathematical formula is not directed to the type of subject matter eligible for patent protection. If USPTO personnel determine that the claimed invention preempts a 35 U.S.C. 101 judicial exception, they must identify the abstraction, law of nature, or natural phenomenon and explain why the claim covers every substantial practical application thereof (see, MPEP 2106, IV C2).

The language of the claim raises a question as to whether the claim is directed merely to an abstract idea that is not tied to a technological art, environment or machine which would result in a practical application producing a concrete, useful, and tangible result to form the basis of statutory subject matter under 35 U.S.C. 101.

The claimed invention as a whole must accomplish a **practical application**. That is, it must produce a **"useful, concrete and tangible result."** *State Street*, 149 F.3d at 1373, 47 USPQ2d at 1601-02. MPEP 2106.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Jain (US Patent No: 6,853,597).

Regarding independent Claims 1, 7, 13, 17, Jain discloses a method and apparatus for an integrated circuit, IC 100, having a BIST control unit 102 for testing a plurality of memory banks (104a-d) simultaneously, see Summary of the Invention and Fig. 1, comprising:

Selecting a bit (faulty word, BitF) included in the test results (TR) during the BIST test mode from each of the plurality of memory banks (104a-d) formed on the IC chip 100, Figs. 1-4.

Selecting one of the memory banks (104a-d) using bank select signal (Sel) included in the test control signals TC.

Storing each selected bit (faulty word, BitFa-d) from each of the plurality of memory banks (104a-d) in the BIST control unit 102, Fig. 1. The memory data

MemData is subsequently compared to the test pattern (TData) supplied by the BIST control unit. In one embodiment, the results of the comparison sBitF are passed to the test control unit and stored in, for example, a buffer. The results from a plurality of test runs are combined using, for example, a logical OR circuit to generate the final results BitF. The final results BitF are output to the BIST control unit with the corresponding addresses Add, Fig. 3.

Regarding Claims 2, 3, 8, 9, Jain discloses selecting a bit from each of the memory banks (104a-d) includes selecting (word lines 214 and 216) interconnecting the memory cells, the memory cell comprising a first port 206 and a second port 208 coupled to a row decoder 218, Fig. 3, by accessing the memory performed through the first port or the second port. The first port is accessed by selecting the appropriate first word line and first bit line and the second port is being accessed by selecting the appropriate second word line and second bit line.

Regarding Claims 4, 5, 10, 11, Jain discloses storing the selected bit from the selected memory banks (104a-d) includes storing each selected bit (faulty word, BitFa-d) from each of the plurality of memory banks (104a-d) in the BIST control unit 102, Figs. 1-3.

Regarding Claims 6, 12, Jain discloses BIST control unit 102 provided to test the plurality of memory banks 104a-d simultaneously. Various input signals, such as the clock signal CLK and activation signal TStart, are provided to the BIST control unit. The clock signal CLK provides the timing for operations such as the transmission of data, and the activation signal TStart activates the BIST control unit during test mode.

Regarding Claims 14-16, 18-21 Jain discloses decoder 218, including decoding logic and word line drivers coupled to the first word lines. The decoding logic receives a first row address (RA), decodes it, and activates the word line driver coupled to the word line corresponding to the decoded address. A column decoder receives a column address CA and selects an output signal of the appropriate sense amplifier, and forwards it to interface circuitry 227. The interface circuitry 227 transfers data read from the selected cell to, for example, a data-out bus (DO), Fig. 3.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques H. Louis-Jacques can be reached on (571) 272-4150. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Date: 27 September 2007
Office Action: Non-Final Rejection

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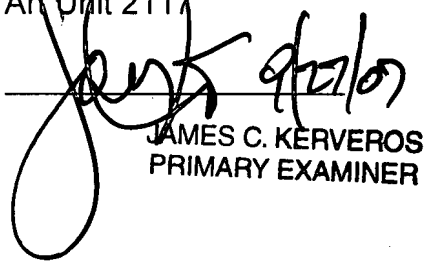

JAMES C. KERVEROS
PRIMARY EXAMINER